**DRAWINGS**

Applicant submits herewith:

- one replacement sheet of Figure 13 and

- one replacement sheet of Figure 14.

The replacement sheets of Figs. 13 and 14 show the location of $V_{gn}$.

The addition of $V_{gn}$ is believed to be fully supported by the original disclosure, as explained in the Remarks below.

## REMARKS

Clams 1-10 are pending in the application. By this Amendment, new claims 5-10 are added.

Claims 2-4 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Claims 1 and 3 are rejected under 35 U.S.C. § 102(b) as being anticipated by Wu et al. (U.S. Patent No. 5,307,007; hereinafter "Wu"). Claims 1 and 3 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu in view of Applicant's Prior Art (Fig. 1) (hereinafter "APA"). Claim 2 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu in view of APA or Yamazaki (U.S. Patent No. 5,180,967; hereinafter "Yamazaki"). Claims 1-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of Wu. Applicant submits the following in traversal of the claim rejections.

Rejections of Claims 2-4 § 112, first paragraph

Applicant submits that claims 2-4 comply with 35 U.S.C. § 112, first paragraph and that the changes to Figs. 13 and 14 are supported by the original disclosure, including the originally filed claims.

For example, the combination of the originally filed claims, paragraphs 56-58 and the related discussion of $V_{gn}$ in Fig. 7 in paragraphs 43-47 provide support for the changes to Figs. 13 and 14.

Rejection of Claims 1 and 3 under § 102(b) by Wu

Applicant respectfully submits that claim 1 is believed to be patentable for reasons previously noted in the Appeal Brief, that:

First, this particular node at the gate of NMOS transistor M3 cannot correspond to the claimed output node. This particular node is merely connected to the gate of PMOS transistor M1, the gate of the NMOS transistor M3, the gate of the NMOS transistor M4, the capacitor $C_1$ and the source/drains of the NMOS transistor M3 and M4. Therefore, there is no way for this particular node to provide any sort of output, and thus, cannot possibly correspond to the claimed output node.

For reasons similar to those submitted for claim 1, Applicant argues that claim 3 is believed to be patentable.

Rejection of Claims 1 and 3 under § 103(a) over Wu in view of APA

Applicant respectfully submits that a *prima facie* case of obviousness has not been established for claim 1. In the Office Action, the Examiner alleges that it would have been obvious for one skilled in the art to add the output node REF as disclosed in Fig. 1 of the present application, to the drain of M3 of Wu. The motivation supplied by the Examiner, however, is "for the benefit of conveying an output signal to the next circuit M5/M6 as shown."

Applicant respectfully submits that this motivation is not supportable because Fig. 1 of Wu shows the drain of M3 as being *already* connected to the circuit formed by M5/M6. Therefore, the Examiner's motivation to combine the teachings of Wu and APA is without merit.

For reasons similar to those submitted for claim 1, claim 3 is believed to be patentable.

Rejection of Claim 2 under § 103(a) over Wu in view of APA or Yamazaki

Applicant submits that a *prima facie* case of obviousness has not been established for claim 2. The Examiner argues that it would have been obvious "to move the resistor R1

[disclosed in Fig. 1 of Wu] from the source of the first PMOS transistor to the source of the second NMOS transistor as taught by [APA] or Yamazaki Fig. 1." The motivation for this modification would be for the "benefit of providing an alternate equivalent circuit layout." Again, Applicant argues that this motivation relies on improper hindsight and that the Examiner relies on a circular argument, i.e., the reason to modify the circuit of Wu is to provide a modified circuit ("for the benefit of providing an alternative equivalent circuit layout").

Rejection of Claims 1-4 under § 103(a) over Yamazaki in view of Wu

Applicant respectfully submits that claims 1-4 are believed to be patentable for the arguments in the Appeal Brief, that:

> In addition, Yamazaki and Wu do not expressly disclose the claimed output node. Although the Examiner mentions nodes N11 or N12 of Yamazaki, there is nothing in Yamazaki that suggests that these nodes correspond to the claimed output node. Instead, the node N11 is connected to the drain and the gate of the PMOS 104, the gate of the PMOS 106, the gate of the PMOS transistor 116, the drain of the NMOS transistor 118, and the drain of the NMOS transistor 112. Node N12 is connected to the drain of the PMOS transistor 105, the drain of the PMOS transistor 120, and the gate and the drain of the NMOS transistor 110. Yamazaki fails to disclose the claimed output node and, thus, claim 1 is believed to be patentable.

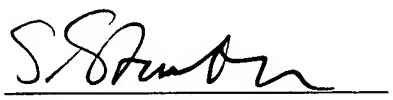
Lastly, Applicant submits new claims 5-10 to more fully claim the invention. The new claims 5-8 are believed to be patentable at least by virtue of their dependencies and new

independent claim 9 and dependent claim 10 are believed to be patentable for reasons similar to those submitted for claims 1 and 3.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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